REMARKS

The specification has been amended to overcome the objection of the Examiner.

The claims have been amended to overcome the objection of the Examiner, and the rejection of claims 6-9 under 35 U.S.C. §112, second paragraph.

Claim 1 was rejected under 35 U.S.C. §102(b) as being anticipated by Hiramoto et al., (U.S. Patent No. 5,661,329). Claims 2-10 were rejected as being unpatentable under 35 U.S.C. §103(a) as being unpatentable over Hiramoto et al. in view of Nii et al., (U.S. Patent No. 5,933,719). Claim 1 provides that the annular diffused region, placed between the first annular isolation trench and the second isolation trench, has a second conductivity-type, in contrast to the collector well which has a first conductivity-type. In the Office Action, the Examiner alleges that element 2 in Hiramoto et al. is equivalent to the annular diffused region of claim 1, and the Examiner also alleges that element 2 in Hiramoto et al. is also equivalent to the collector well of claim 1, (Office Action, paragraph 1). This implies that the annular diffused region, being a part of the collector well in Hiramoto et al., namely, being part of element 2, has the same conductivity-type as the collector well, namely, a first conductivity-type, but claim 1 indicates that the annular diffused region has a second conductivity-type different from the first conductivity-type of the collector well.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**"

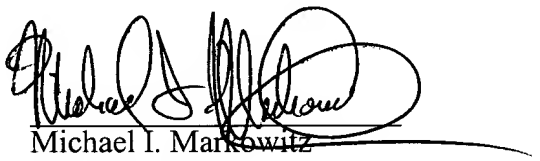
CLOSING

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claim 1 is in condition for allowance, as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,



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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph on page 7, lines 5-15, have been rewritten as follows:

The present invention provides a semiconductor device including a silicon substrate, and a bipolar transistor having a collector well having a first conductivity-type, an intrinsic base region having a second conductivity-type and received in the collector well and an emitter region having the first conductivity-type and received in the intrinsic base region, a first annular isolation trench encircling the collector well, a second annular isolation trench encircling the first annular isolation trench, and an annular diffused region disposed between the first annular isolation trench and the second isolation trench while being in contact with the first and second isolation trenches.

The paragraph on page 14, lines 1-11, has been rewritten as follows:

The first annular isolation trench 20b for the NPN bipolar transistor 12 encircles an n-well or collector well 22 constituting the collector region of the NPN transistor 12. For the NPN bipolar transistor 12, an annular p-well 21 is disposed between the first annular isolation trench 20a and the second annular isolation trench 20b for encircling the collector well 22. The p-well [12] 21 functions for isolation by forming a p-n junction between the same and the collector well 22. The annular p-well 21 has an inner edge defined by the outer edge of the first annular isolation trench 20a and an outer edge defined by the inner edge of the second annular isolation trench 20b.

IN THE CLAIMS

Claims 1, 2 and 6 have been rewritten as follows:

1. (Once Amended) A semiconductor device comprising a silicon substrate, and a bipolar transistor having a collector well having a first conductivity-type, an [intrinsic] internal base region having a second conductivity-type and received in said collector well and an emitter region having said first conductivity-type and received in said [intrinsic] internal base region, a first annular isolation trench encircling said collector well, a second annular isolation trench encircling said first annular isolation trench, and an annular diffused region having said second conductivity-type disposed between said first annular isolation trench and said second annular isolation trench while being in contact with said first and second annular isolation trenches.

2. (Once Amended) The semiconductor device as defined in claim 1, wherein said [intrinsic] internal base region and said collector well are provided with a base electrode and a collector electrode, and each of said base electrode, said collector electrode and said annular diffused region is provided with a silicide layer on top thereof.

6. (Once Amended) The semiconductor device as defined in claim [6,] 1, wherein said silicon substrate has said second conductivity-type.